AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (currently amended): A method of fabricating a trench device structure with a single-side buried strap, comprising the steps of:

providing a semiconductor substrate having a deep trench therein;

forming a buried trench capacitor in a lower portion of the deep trench;

forming a collar insulating layer lining an upper portion of the deep trench;

forming a first conductive layer overlying the buried trench capacitor in the trench and surrounded by and lower than the collar insulating layer by a predetermined height;

removing a first portion of the collar insulating layer from the deep trench to expose a first portion of the semiconductor substrate while a second portion of the collar insulating layer remains to isolate a second portion of the semiconductor substrate;

forming a second conductive layer overlying the first conductive layer in the deep trench, wherein the second conductive layer is lower than the surface of the semiconductor substrate and a portion of the second conductive layer is isolated from the semiconductor substrate by the second portion of the collar insulating layer; and

forming the single-side buried strap region in the semiconductor substrate directly contacting the second conductive layer without isolation by the collar insulating layer.

Claim 2 (Previously presented): The method as claimed in claim 1, removal of the first portion of the collar insulating layer from the sidewall of the deep trench further comprising:

sequentially forming a conformal lining layer and an undoped polysilicon or amorphous silicon layer on the surface of the semiconductor substrate and inner surface of the deep trench above the second conductive layer;

performing a tilt ion implantation on the undoped polysilicon or amorphous silicon layer, wherein a portion of the undoped polysilicon or amorphous silicon layer in the deep trench is not implanted;

selectively wet etching the undoped polysilicon or amorphous silicon layer, thereby exposing the underlying lining layer;

sequentially etching the exposed lining layer and the contiguous collar insulating layer to expose a portion of the semiconductor substrate using the doped polysilicon or amorphous silicon layer as a mask; and

removal of the remaining lining layer and the doped polysilicon or amorphous silicon layer.

Claim 3 (Original): The method as claimed in claim 2, wherein the lining layer is composed of silicon nitride.

Claim 4 (Original): The method as claimed in claim 3, wherein the thickness of the silicon nitride is approximately 100Å.

Claim 5 (Original): The method as claimed in claim 3, wherein the undoped polysilicon or amorphous silicon layer and the silicon nitride lining layer are formed by low pressure chemical vapor deposition (LPCVD).

Claim 6 (Original): The method as claimed in claim 2, wherein the thickness of the undoped polysilicon or amorphous silicon layer is between 50 and 100Å.

Claim 7 (Original): The method as claimed in claim 2, wherein the dopant of the tilt ion implantation is BF_2 or B.

Claim 8 (Original): The method as claimed in claim 7, wherein the tilt angle of the ion implantation is 7° to 15°.

Claim 9 (Original): The method as claimed in claim 7, wherein the etching solution of the selectively wet etching is low concentration ammonia solution.

Claim 10 (Original): The method as claimed in claim 2, removal of the remaining lining layer and the doped polysilicon or amorphous silicon layer further comprising:

oxidation of the remaining doped polysilicon or amorphous silicon layer; and

sequential removal of the oxidized polysilicon or amorphous silicon layer and the underlying lining layer.

Claim 11 (Original): The method as claimed in claim 1, wherein the collar insulating layer is composed of tetra ethyle ortho silicate (TEOS) formed by chemical vapor deposition (CVD).

Claim 12 (Original): The method as claimed in claim 11, wherein the thickness of the collar insulating layer is from 200 to 300Å.

Claim 13 (Original): The method as claimed in claim 1, wherein the first and second conductive layers are composed of doped polysilicon.

Claim 14 (Original): The method as claimed in claim 13, wherein the buried strap region in the semiconductor substrate is formed by a thermal treatment.

Claim 15 (Original): A method of fabricating a trench device structure with a single-side buried strap, comprising the steps of:

providing a semiconductor substrate having a pad layer thereon and a deep trench therein;

forming a buried trench capacitor in a lower portion of the deep trench;

forming a collar insulating layer lining an upper portion of the deep trench

forming a first conductive layer overlying the buried trench capacitor in the trench and surrounded by and lower than the collar insulating layer by a predetermined height;

sequentially forming a conformal lining layer and an undoped polysilicon or amorphous silicon layer on the surface of the pad layer and inner surface of the deep trench above the first conductive layer;

performing a tilt ion implantation on the undoped polysilicon or amorphous silicon layer, wherein a portion of the undoped polysilicon or amorphous silicon layer in the deep trench is not implanted;

selectively wet etching the undoped polysilicon or amorphous silicon layer, thereby exposing the underlying lining layer;

sequentially etching the exposed lining layer and the contiguous collar insulating layer to expose a portion of the semiconductor substrate using the doped polysilicon or amorphous silicon layer as a mask;

removal of the remaining lining layer and the doped polysilicon or amorphous silicon layer;

forming a second conductive layer overlying the first conductive layer in the deep trench, wherein the second conductive layer is lower than the surface of the semiconductor substrate; and

performing a thermal treatment to form a buried strap region on the semiconductor substrate directly contacting the second conductive layer without isolation by the collar insulating layer.

Claim 16 (Original): The method as claimed in claim 15, wherein the lining layer is composed of silicon nitride.

Claim 17 (Original): The method as claimed in claim 16, wherein the thickness of the silicon nitride is approximately 100Å.

Claim 18 (Original): The method as claimed in claim 16, wherein the undoped polysilicon or amorphous silicon layer and the silicon nitride lining layer are formed by low pressure chemical vapor deposition (LPCVD).

Claim 19 (Original): The method as claimed in claim 15, wherein the thickness of the undoped polysilicon or amorphous silicon layer is between 50 and 100Å.

Claim 20 (Original): The method as claimed in claim 15, wherein dopant of the tilt ion implantation is BF_2 or B.

Claim 21 (Original): The method as claimed in claim 20, wherein the tilt angle of the ion implantation is 7° to 15°.

Claim 22(Original): The method as claimed in claim 20, wherein the etching solution of the selectively wet etching is low concentration ammonia solution.

Claim 23-29 (Canceled)